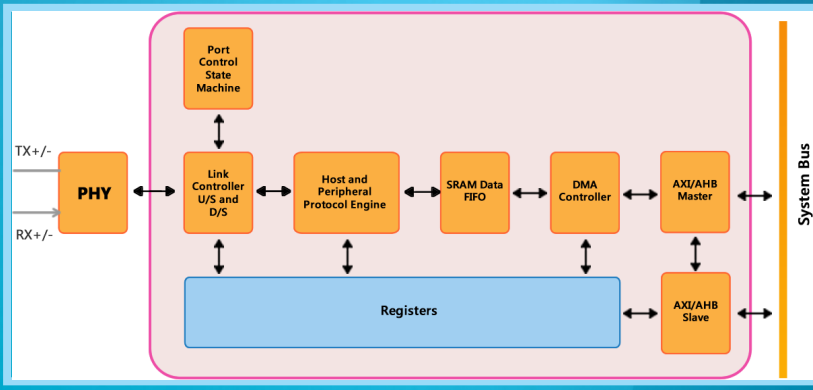
Inno-Logic
ASIC.FPGA.Embedded

USB 3.0 SuperSpeed OTG

Overview

Innovative Logic SS-OTG controller IP is complaint with OTG&EH3.0. SS-OTG controller is able to dynamically swap host/peripheral roles while operating at Super-Speed using Role Swapping Protocol (RSP) as defined in OTG&EH3.0 specification. The IP is capable of handling multiple devices when acting as Host.



Features

- Compliant with:
  - USB3.0 specification
  - OTG&EH3.0 specification
- USB3.0 PIPE interface
  - Support 8/16/32 data bus width
- AXI, AHB, PLB Bus standards
  - Support 32/64 bit data bus
- Supports RSP – Role Swap Protocol
- Hub Class support and supports multiple System bus interfaces – AXI/AXI/PLB with 32/64 bit data bus
- Supports Super Speed OTG communication
- Support USB3 power down modes
- Support Control, Bulk, Isochronous and Interrupt transaction
- Configurable up to 15 transmit and 15 receipt endpoints apart from default endpoint
- Dynamically configurable Endpoint FIFO for optimum usage of memory
- Synchronous SRAM interface for FIFO
- Integrated DMA controller

Target Applications

- Removable hard disks
- Digital camera
- Printer, scanner etc
- Multimedia Applications
- Mobile phones and Tablets
- TV, DVD players, Set top Boxes

Deliverables

- Synthesizable RTL developed in Verilog
- Constraints for synthesis
- Test bench and Test cases developed using System Verilog
- Documentation

Functional Description

Port Control State Machine:
This tracks the events at the port for any successful attachment and detachments. This manages both SS and HS/FS ports.

Link Controller:
Link Layer consists of blocks which is responsible for the controlling link and port functionality. All link level protocol controlling is handled by this block. It also has PIPE interface logic. It manages low power mode entry and exits.

Protocol Engine Host and Peripheral function:
This layer handles the USB protocol both in Host and Peripheral mode. In Peripheral mode it handles all the transactions directed towards configured Endpoints. In the Host mode it initiates all the USB transactions. Protocol layer handles concurrent IN and OUT transactions in both Peripheral and Host modes.

DMA Controller:
The core has integrated DMA controller which enables the data transfer between Endpoint Data FIFO and the System Memory. Endpoint Data FIFO is realized using dual port SRAM.

Bus Interface:
System Bus slave interface enables easy integration of core in any system. Bus Master tightly linked to DMA controller enables the DMA to work as Master. Bus interface support AXI/AHB/PLB bus **protocols.**

Corporate Headquarter and North America Design Center

Innovative Logic Inc.
1731 Technology Dr,
Suite.#550
San Jose, CA 95110

Phone: (408)824-1313
Fax: (408)418-4056
Email: info@inno-logic.com

Asia Pacific Design Center
Innovative Logic Pvt Ltd.

96/112, II Floor, Bull Temple Road,
Bangalore - 19, Karnataka, INDIA
Phone: +91-80-5770 2835
VOIP: (408)856-6121
Email: info@inno-logic.com