Inno-Logic
ASIC.FPGA.Embedded

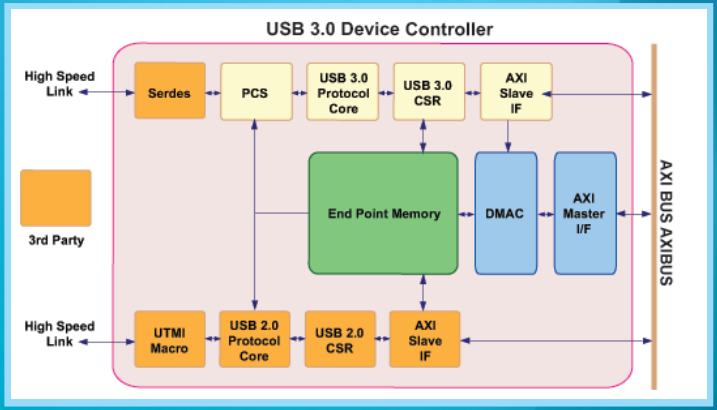
USB 3.0 SuperSpeed Device Controller

Overview

USB 3.0 device controller is designed to be used in a system to provide Super High speed USB connectivity between the device it is being used and the USB host.

This IP is designed based on the USB 3.0 specification 1.0. It is able to interface with industry standard AMBA AXI bus. This makes this IP easily integrated in any SOC that has one of this industry standard bus architecture.

This IP is being developed using Verlilog HDL and verified using SystemVerilog.



Features

- Compliant with USB3.0 Specification rev1.0
- Compliant with USB 3.0 PIPE interface for seamless
- integration with PHY
- Supports 16 bit USB PIPE interface at 250 MHZ PHY
- clock
- MAC Capable of scrambling/descrambling
- Supports LFPS for initialization and power management
- Supports separate clocking for Application layer
- Depth and position of endpoint buffers is configurable
- Size of endpoint buffer of each endpoint is configurable
- Separate Endpoint Buffers for IN bound and OUT bound
- data packets
- Supports full power management
- AXI & AHB Interface support on application side
- Contain 1 Control endpoint
- Support 16 IN &16 OUT functional endpoints
- All endpoints supports all type of data transfer – Bulk,
- ISO, Interrupt, Control.
- Endpoint type configurable through software
- Bulk endpoints support Bulk Streaming
- Fully Integrated DMA controller for data transfer
- between EP buffer and system memory
- Programmable DMA enable/disable feature
- Programmable hardware/software request for each
- DMA channel
- DMA supports both increment and decrement addressing
- mode

Target Applications

- Removable hard disks
- Digital camera
- Printer, scanner etc
- Multimedia Applications

Deliverables

- Fully Synthesizable RTL code
- SystemVerilog based verification environment
- Synthesis constraints and scripts files
- User Manual and verification document
- Programmer model document
- Synthesis constraints and scripts files

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