**General Description**

Innovative Logic USB3.1 Gen2 (SSP) Device Controller IP is compliant with USB3.1 Gen2 standard. It supports Gen2 at 10Gbps, Gen1 at 5Gbps and is fully backward compatible with USB2.0 protocol.

Innovative Logic SSP Device controller IP supports 15 IN and 15 OUT functional endpoints along with a default control endpoint.

Each endpoint is capable of carrying out Bulk, Isochronous or Interrupt transaction. Endpoint type is set through firmware. Bulk endpoints additionally support Bulk Streaming protocol.

Innovative Logic SSP controller IP supports AXI and AHB system bus interfaces and supports 32/64/128 bit data bus.

**Features**

- Compliant with:
  - USB3.1 Gen 2 specification
  - USB3.1 PIPE interface
  - Support 32/64 data bus width
  - AXI, AHB Bus standards
  - Supports 32/64/128 bit data bus
- Supports all USB3.1 power down modes
- Supports Control, Bulk, Isochronous and Interrupt transaction
- Bulk endpoint support streaming
- Device can be configurable up to 15 IN and 15 OUT functional endpoints
- Configurable number of function endpoints
- Dynamically configurable Endpoint FIFO for optimum usage of memory
- Synchronous SRAM interface for FIFO
- Fully integrated DMA controller

**Block Diagram**

Block Diagram of USB 3.1 Gen2 Device Controller
Details

**USB3.1 Gen1/2 Link Controller**

USB3.1 Gen1&Gen2 Link layer is implemented in this block. It manages link training, link level data traffic and power modes. It supports both Gen1 and Gen2 speeds. It communicates with PHY using USB3.1 PIPE interface.

**USB3.1 Gen1/2 Protocol Core**

This handles complete USB3.1 Gen1&Gen2 protocol functionality. It handles all types of protocol packets. This block also includes Endpoint FIFO controller.

**USB3.0 and USB2.0 CSR**

These blocks have all the Control and Status Registers. Firmware uses control registers to control the core. Status registers provide controller status. There are also many registers that may be used for debugging.

**USB2.0 Protocol Core**

This handles complete USB2.0 protocol functionality. It handles all types of protocol packets and retries. This also includes Endpoint FIFO controller. It communicates with PHY using USB2 UTMI/ULPI interface.

**Bus Slave Interface**

This provides System Bus access. This supports AXI and AHB bus. Data width supported is 32/64/128. System controller can access registers through this interface.

**DMA Controller and Bus Master Interface**

This is fully integrated DMA controller. It comes with Bus Master Interface. It supports AXI and AHB System bus with 32/64/128 bit data width. It is closely coupled with Endpoint FIFO for efficient data transfer.

Target Applications

- Removable hard disks
- Digital camera
- Printer, scanner, etc.
- Multimedia Applications
- Mobile phones and Tablets
- TV, DVD players, Set top Boxes

Key Benefits

- Optimized designed to achieve lowest power and area for portable electronics
- Extensive debug capabilities
- Configurable options to tune the core as per requirement

Deliverables

- Synthesizable RTL developed in Verilog HDL
- Constraints & scripts for synthesis
- Test bench and Test cases developed in SystemVerilog
- Sample Driver code
- User Manual

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