Inno-Logic
INNOVATIVE LOGIC INC.

USB 2.0 High Speed Device Controller

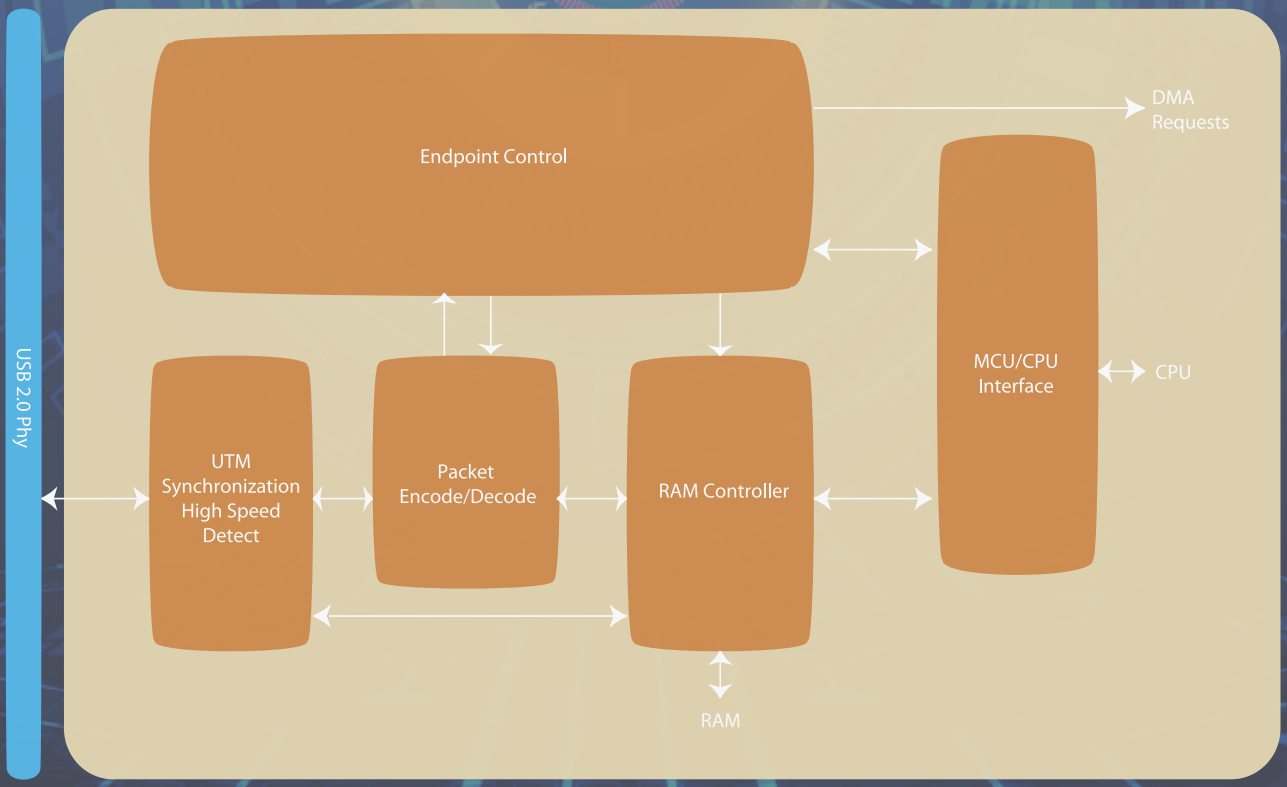
General Description

Innovative Logic's USBHSFC core provides a USB device controller that conforms to the USB 2.0 specification for Hi-/Full-Speed (480/12 Mbps) functions. The USBHSFC has a RAM interface for connecting to a single block of synchronous single-port RAM. The USBHSFC provides a USB 2.0 Transceiver Macrocell Interface (UTMI) to connect to an 8/16-bit Hi-/Full-Speed transceiver. Access to the FIFOs and internal control/status registers may be via a 16/32-bit AMBAAHB-compatible synchronous CPU interface via the AMBAAHB bridge. The USBHSFC has a RAM interface for connecting to the single block of synchronous RAM that is used for all the Endpoint FIFOs. The device also offers support for DMA access to the Endpoint FIFOs. The device also offers support for DMA access to the Endpoint FIFOs. (The USBHSFC-AHB bridge includes DMA controller hooks.)

Features

- Complies with the latest USB 2.0 standard for Hi-Speed (480 Mbps) and Full-Speed (12 Mbps)
- Configurable up to 15 additional IN or OUT Endpoints
- Configurable FIFO sizes from 8 to 8,192 bytes with option of dynamic FIFO sizing
- UTMI: USB Transceiver Macrocell Interface
- Built-in 16/32-bit synchronous AMBA AHB-compatible CPU interface
- Support for DMA access to FIFOs
- Synchronous RAM interface for FIFOs
- Supports suspend and resume signaling
- Fully synthesizable
- Scan test ready

Block Diagram



Block Diagram of USB 2.0 High Speed Device Controller

USB 2.0 High Speed Device Controller

Details

Structure

The MUSBHSFC function controller consists of a UTM re-synchronizing block, a packet encoder/decoder plus CRC generator/checker block, RAM controller, MCU interface, plus a control block for each Endpoint. The function controller interfaces to a UTMI v1.04 USB 2.0 transceiver macrocell.

USB Transceiver Macrocell (UTM) Sync Block

The role of this block is to resynchronize between the trans-ceiver macrocell (30/60 MHz clock domain) and the function controller's user-supplied clock (>30 MHz). This allows the rest of the MUSBHSFC to run from the bus clock without requiring any further synchronization. If an 8-bit transceiver interface is configured, this block will convert the data to 16-bit so that a user clock down to 30 MHz can be utilized. The block also performs the Hi-Speed detection handshaking.

MCU/CPU Interface

The core may be integrated to a range of different CPU bus standards. The interface provided by the USBHSFC is a 16/32-bit synchronous AMBAAHB-compatible CPU interface.

Packet Encoder/Decoder

The packet encoder/decoder block generates headers for packets to be transmitted and decodes the headers of received packets. It also performs CRS generation and checking.

Endpoint Controllers

Utilizes two controller state machines, 1 for control transfers over EP0, and 1 for bulk/interrupt/isochronous transactions EP1-15

RAM Controller

The RAM controller provides an interface to a single block of synchronous RAM, which is used to buffer packets between the MCU and the USB. It takes the FIFO pointers from the Endpoint controllers, converts them to address pointers within the RAM block and generates the RAM access signals.

Target Applications

- Removable hard disks
- Digital camera
- Printer, scanner, etc.
- Multimedia Applications
- Mobile phones and Tablets
- TV, DVD players, Set top Boxes

Deliverables

- Synthesizable RTL developed in Verilog HDL
- Constraints & scripts for synthesis
- Test bench and Test cases developed in SystemVerilog
- Sample Driver code
- User Manual

Key Benefits

- Optimized designed to achieve lowest power and area for portable electronics
- Extensive debug capabilities
- Configurable options to tune the core as per requirement

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