Inno-Logic
INNOVATIVE LOGIC INC.

USB 3.1 Gen2 Host Controller

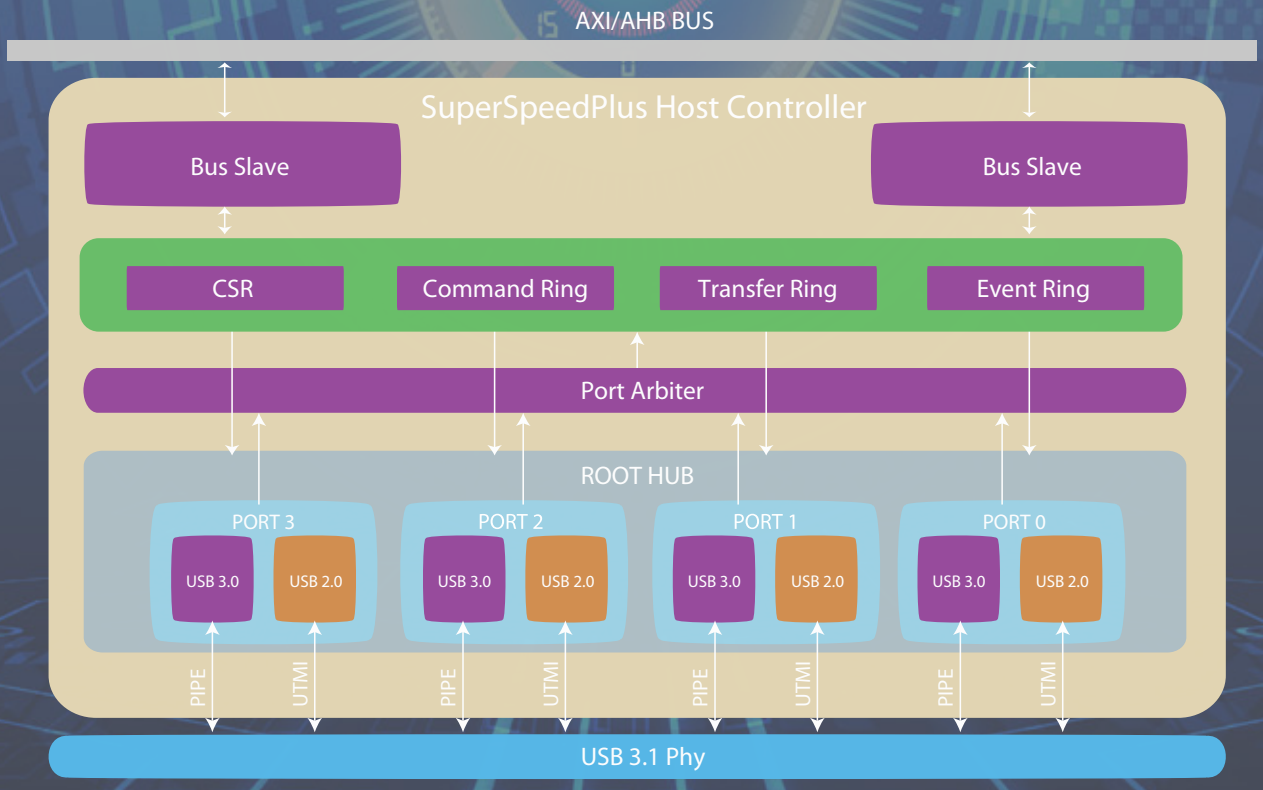
General Description

Innovative Logic's SuperSpeedPlus Host controller IP is a standard USB Host controller IP. It is fully compliant with xHCI specification and USB3.1 specification. It is also backward compatible with USB2.0 specification. The Host controller supports all types of USB devices and transactions. It supports multiple root hub ports and capable of handling multiple devices including hubs. Innovative Logic's Host controller supports many configuration features helping user to mould the IP as per their requirement. Innovative Logic's Host controller IP supports AXI and AHB system bus interfaces with support to 32/64/128 bit data bus width. The Host controller IP supports PIPE and UTMI interface for easy integration with PHY IP.

Features

- Compliant with:
  - xHCI specification
  - USB3.1 specification
  - USB3.1 PIPE interface
    - Support 8/16/32 data bus width
  - UTMI interface
    - Support 8/16 data bus width
  - AXI, AHB Bus standards
    - Supports 32/64/128 bit data bus
- Support multiple root hub ports
- Support multiple Devices and Endpoints
- Supports many configuration options
- Supports all USB3 power down modes
- Supports all types of US transaction including Bulk Streaming
- Synchronous SRAM interface for FIFO
- Fully integrated DMA controller

Block Diagram



Block Diagram of USB 3.1 Gen2 Host Controller

USB 3.1 Gen2 Host Controller

Details

USB3.1 Port Block

This block supports USB 3.1 Link Layer and Protocol Layer Functionality. It also contains xHC port register functionality USB3.1 Link layer contains LTSSM. It manages link training and handles link level data traffic and power modes. It communicates with PHY using USB3 PIPE interface

USB3.1 Protocol Layer

Handles bulk, iso, interrupt and control transactions. It maintains Endpoint FIFO. xHC block fetches transfer, command ring TRBs, decodes and then executes before fetching the next TRB. Arbitration logic selects specific ring for processing from outstanding doorbell rings. This block supports multiple interrupters. Event ring manager prepares event ring and submits the write request.

USB3.0 and USB2.0 CSR

These blocks have all the Control and Status Registers.

USB2.0 Protocol Core

This handles complete USB2.0 protocol functionality. In device mode it handles all types of protocol packets. In Host mode, it initiates transactions if it is requested by scheduler. This also includes Endpoint FIFO controller. It communicates with PHY using USB2 UTMI/ULPI interface.

Bus Slave Interface

This provides System Bus access. This support AXI and AHB bus. System controller can access registers through this interface.

Bus Master Interface

It comes with Bus Master Interface. It handles requests from multiple clients for memory read and write access

Target Applications

- Removable hard disks
- Digital camera
- Printer, scanner, etc.
- Multimedia Applications
- Mobile phones and Tablets
- TV, DVD players, Set top Boxes

Deliverables

- Synthesizable RTL developed in Verilog HDL
- Constraints & scripts for synthesis
- Test bench and Test cases developed in SystemVerilog
- Sample Driver code
- User Manual

Key Benefits

- Optimized designed to achieve lowest power and area for portable electronics
- Extensive debug capabilities
- Configurable options to tune the core as per requirement

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